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Control of surface morphology and crystal structure of silicon nanowires and their coherent phonon transport characteristics

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Abstract

We report on the first experimental observation of coherent phonon transport characteristics in silicon nanowires (SiNWs) synthesized by a one-step surface reconstruction growth mechanism. As-grown SiNWs taper down along the growth direction alongside a decrease in both roughness and stacking fault density. Furthermore, by systematically measuring the temperature-dependent thermal conductivity using a conventional thermal bridge method, we found that the measured thermal conductivity values of surface-reconstructed (SR)-SiNWs (13–20 $W\,m^{-1}\,K^{-1}$) at room temperature are markedly lower than that predicted from the conventional diffuse phonon transport model for given NW diameters. We also observed that the thermal conductivities of SR-SiNWs exhibit an unexpected power law of $\sim T^{\alpha}$ ($1.6 \leqslant \alpha \leqslant 1.9$) in the temperature range of 25–60 K, which cannot be explained by the typical Debye $\sim T^{3}$ behavior. Interestingly, our experimental results are consistent with a frequency-dependent model, which can be induced by coherence in the diffuse reflection and backscattering of phonons at the rough surface and stacking faults on SR-SiNWs, resulting in the suppressed thermal conductivity. Therefore, the demonstrated rational synthesis model and measurement technique promise great potential for improving the performance of a wide range of one-dimensional NW-based thermoelectric devices.

Keywords: Silicon nanowires; Thermal conductivity; Stacking fault; Phonon boundary scattering; Coherent phonon transport

1. Introduction

Over the past few years, a number of research groups have intensively studied, both experimentally [1–5] and theoretically [6–10], the enhancement of thermal properties (figure-of-merit; ZT) of silicon nanowires (SiNWs), primarily focusing on diameter reduction and surface roughness. Of particular importance in the application of SiNWs to thermoelectric (TE) devices [11,12] is the need to reduce the effective thermal conductivity of the NW through enhancement of phonon-boundary scattering at rough surfaces and/or interlayers, which can act as important phonon scattering interfaces. Control over the surface morphology (roughness and facets), crystal structure and crystalline defects in SiNWs can provide a route to the reduction of thermal conductivity via diffuse reflection

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and backscattering. The Yang and Majumdar [1,3,4] research groups have used metal-catalyzed vapor–liquid–solid (VLS) growth and the wet chemical etching process to show that the thermal properties of thin and rough SiNWs can be improved 100-fold relative to that of bulk Si. More recently, Sansoz [10] showed by molecular dynamics (MD) simulations that the thermal conductivity is greatly reduced in crystalline ⟨1 1 1⟩ SiNWs having periodic sawtooth faceting compared to those for smooth SiNWs with the same dimensions, thus providing a strategy to optimize the design and performance of SiNWs as TE elements.

To date, several research groups have documented faceting on SiNW sidewalls in the VLS growth process. Recently, Hannon et al. [13] observed nanoscale faceting in SiNWs during Au-catalyzed VLS growth in ultra-high vacuum, and reported that facets on the SiNW sidewalls were created by the interplay of Au diffusion from Au–Si droplets and a subsequent vapor–solid (VS) process with increasing growth time. den Hertog et al. [14] also reported that diffusion of Au in SiNWs could be controlled by silane partial pressure and growth temperature. More recently, Oehler et al. [15] found that the presence of Au on SiNW sidewalls has a critical effect on its morphology because Au diffusion along the sidewalls causes surface reconstruction, which in turn leads to faceting.

However, there have been no systematic studies on the formation, and the resulting phonon transport characteristics, of ⟨1 1 1⟩-oriented stacking faults on/in {1 1 1}/{1 0 0} SiNW sidewalls facets. In order to enhance phonon scattering in SiNWs, we report in this study a strategy to control the surface morphology and crystal structure of SiNWs by Au-induced VLS–VS growth at a low silane partial pressure. We have observed that surface-reconstructed SiNWs (SR-SiNWs) have not only a rough surface morphology on the sidewalls with {1 1 1}/{1 0 0} faceting, but also stacking faults inside the SiNWs. Moreover, to further elucidate the effects of roughness- and stacking-fault-induced phonon-boundary scattering on coherent phonon transport characteristics in SR-SiNWs, we present systematic experimental studies in terms of roughness, facets and stacking faults using a conventional thermal bridge method over a temperature range of 25–300 K.

2. Experimental

2.1. Synthesis and characterization of SR-SiNWs

The SiNWs were synthesized by an Au-catalyzed hot-wall chemical vapor deposition (CVD) growth mechanism in a quartz-tube thermal furnace with SiH_4 (3% diluted in Ar) as a Si source at a base pressure of 2×10^{-2} torr. Prior to Au-catalyst deposition, a Si wafer was cleaned by buffered hydrofluoric acid (BHF). Au catalyst (~2 nm in thickness) was deposited by e-beam evaporation onto the Si wafer. Then, the Au-coated Si substrates, which have been singulated into 0.7 cm × 0.7 cm dies, were placed into a quartz-tube furnace. The growth experiments were carried out at a pressure of ~3 torr (partial silane pressure of $\sim 8.2 \times 10^{-3}$ torr), a temperature of 550 °C and a SiH_4 flow rate of 3 sccm. The detailed experimental steps are described in our published reports [16,17]. The dimensions, surface morphology, crystal structures and composition of as-synthesized SiNWs were characterized using high resolution scanning electron microscopy (SEM), transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) with energy dispersive X-ray (EDX) analysis. The cross-sectional and longitudinal-sectional specimens for the TEM analysis were prepared using standard procedures in a dual beam focused ion beam (FIB) machine (see details in Fig. S.1 in Supplementary material).

2.2. Microdevice chip, NW manipulation and measurement setup for thermal property measurements

To measure the thermal properties of SiNWs, we used a suspended microdevice chip fabricated by a standard microelectromechanical systems (MEMS) process, as shown in Fig. 1. The fabricated microdevice chip has heating and sensing regions, which were formed by platinum (Pt) coils on silicon nitride (SiN_x) membranes. The local temperature of each membrane can be estimated by measuring the temperature-dependent resistance of the Pt coil. For the placing of a single SiNW between two suspended membranes, a micromanipulator with a tungsten tip was used under an optical microscope. First, as-synthesized SiNWs were rubbed onto a TEM grid, and the tungsten tip was moved near a desired single SiNW on the TEM grid. As a result, the SiNW was naturally attached to the end of the tungsten tip by electrostatic force. Thereafter, we could easily place the SiNW onto the suspended microdevice chip. Additionally, Pt/C composite was also deposited using an e-beam induced deposition (EBID) on the contact regions to reduce the contact thermal resistance between the SiNW and metal electrodes, as shown in Figs. 1 and S.2. The detailed system set-up and procedure for measuring the thermal conductivity of SiNWs are well documented in the literature [1–3,18]. Fig. 2a and b shows the schematic measurement setup of the suspended SiNW

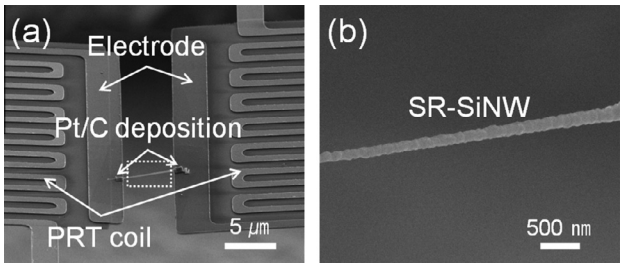

Fig. 1. Microchip for thermal conductance measurement. (a) SEM image of SR-SiNWs placed onto a microdevice chip with Pt/C composite thermal contact by EBID in FIB. (b) Enlarged SEM image of SR-SiNW with rough and tapered surface morphology.

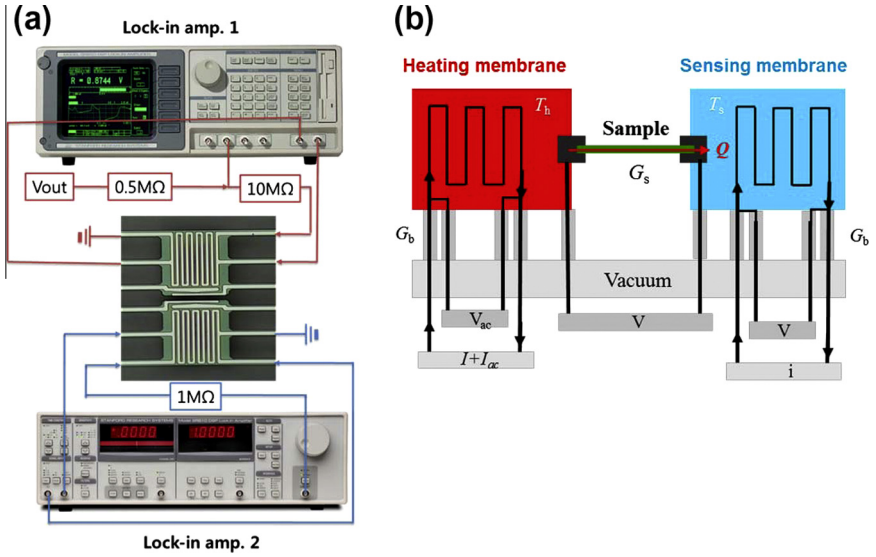

Fig. 2. Thermal conductivity measurement setup and thermal bridge method. (a) Schematic diagram of measurement setup for measuring the thermal conductance of the suspended SiNW using a microdevice chip. (b) Conventional thermal bridge method via a microdevice chip, which is composed of two suspended membranes. It indicates how to determine the thermal conductivity of SiNW suspended membranes.

and a schematic diagram of the thermal bridge method with two suspended membranes for the thermal conductance measurements, respectively. For the thermal conductance measurements, the suspended samples are placed in a cryostat with a vacuum level of $\sim 1 \times 10^{-5}$ torr. As shown in Fig. 2a, the electrical resistances of the sensing and heating membranes are measured using two lock-in amplifiers (SR 830 and SR 850, Stanford research system, USA) with sinusoidal excitation current. All details can be found in previous reports [1,4,18].

2.3. Effective thermal conductivity $\bar{\kappa}$ of taper SiNWs using modified Fourier's law

In this study, the thermal conductivity κ of SiNWs was determined by the conventional thermal bridge method via a microdevice chip, composed of two suspended membranes [1–4,18]. As shown in Figs. 1a and 2b, the floating suspended structure of SiNW should be required to minimize the error of estimated thermal conductivity of SiNW using the thermal bridge thermometer method. For this reason, the heat loss through the substrate can be effectively prevented by the suspended floating structure, and most of the induced heat can flow only through the placed SiNW (Figs. 1a and 2b). The two suspended membranes (Fig. 1a) act as a heater and a sensor, respectively. One membrane (heater) can be Joule heated by AC current to cause heat conduction through the placed SiNW to the other membrane (sensor). Using this technique, we can directly obtain the thermal conductance (G_s) of the SiNW by the following equations [18]:

$$G_b = \frac{Q_h + Q_L}{\Delta T_h + \Delta T_s}, \quad G_s = G_b \frac{\Delta T_s}{\Delta T_h - \Delta T_s} \tag{1}$$

where G_b is the thermal conductance of beams and Q_h and Q_L are the generated Joule heat of heating platinum resistance thermometer (PRT) and Pt leads, respectively. ΔT_h and ΔT_s can be calculated from the measured resistance of the heating and sensing PRTs and their temperature coefficient of resistance (TCR). G_s is the thermal conductance of the placed SiNW onto a platinum resistance thermometer (PRT) formed micro-device chip. The experimentally measured thermal conductance is easily converted into the thermal resistance by taking the inverse of the thermal conductance. The thermal conductivity of the SiNW can also be obtained from G_s. The detailed information for measuring thermal thermoelectric properties of the one-dimensional nanostructures was reported previously [1,18]. From Fourier's law, the thermal conductivity is defined in terms of the thermal current and the temperature gradient:

$$J_x = -\kappa \frac{\partial T}{\partial x} \tag{2}$$

In this definition, κ is the thermal conductivity, J_x is the heat flux per unit area in the x-direction (i.e. along the nanowire) and $\frac{\partial T}{\partial x}$ is the temperature gradient along the x-direction. The intrinsic thermal resistance of a SiNW with the length and geometric cross-section of L and A is given by

$$R_{thermal} = \frac{L}{\kappa A} \tag{3}$$

In this formula, $R_{thermal}$ is the thermal resistance, which is defined by $\Delta T = \dot{Q} R_{thermal}$, where $\dot{Q}$ is the heat generation rate and ΔT is the temperature difference between the ends of the SiNW. The thermal conductivity (κ) is expressed in terms of the experimentally measured quantities as

$$\kappa = L/(AR_{thermal}) = \dot{Q}L/(A\Delta T) = LG_s/A \quad (4)$$

In the case of a tapered SiNW, care should be taken because the geometric cross-section is not constant over the nanowire. To convert the experimentally measured thermal resistance into the thermal conductivity of the tapered SiNW with the length and geometric cross-section of L and $A(x)$, we begin with the definition of the effective thermal conductivity written in the following form:

$$J_x = \frac{\dot{Q}}{A(x)} = -\kappa\frac{\partial T}{\partial x} \quad (5)$$

We integrate the equation with respect to x and obtain

$$\dot{Q}\int_0^L \frac{dx}{\kappa A(x)} = T(0) - T(L) = \Delta T \quad (6)$$

As we noticed from cross-sectional images of tapered SiNW from TEM measurements (Fig. 1b and Fig. S.2 in Supplementary material), the κ is not exactly constant along the nanowire. However, to compare relatively the thermal properties of different sizes of tapered SiNWs, we introduced an effective thermal conductivity ($\bar{\kappa}$), which is assumed to be constant along the nanowire of the sample because the ratio of inner core and outer shell region of tapered SiNW could approximately be a constant along the nanowire and then the result immediately leads to

$$R_{thermal} = \bar{\kappa}\int_0^L \frac{dx}{A(x)} \quad (7)$$

We can easily evaluate the integral with $A(x) = \pi\left(r_B + (r_T - r_B)\frac{x}{L}\right)^2$ and the result is

$$\bar{\kappa} = L/(\pi r_B r_T R_{thermal}) = \dot{Q}L/(\pi r_B r_T \Delta T) = LG_s/(\pi r_B r_T) \quad (8)$$

where r_B and r_T are the radii of the cross-sections at the bottom end and at the top end, respectively.

3. Results and discussion

3.1. Material characteristics of SR-SiNWs

We have successfully grown highly faceted and stacking-faulted SiNWs via Au-catalytic VLS growth. The SiNWs have diameters in the range of 100–200 nm and are up to 10 μm in length, as shown in Fig. 3a. They exhibit not only a typical tapered structure and pronounced facets along the growth direction, but also possess an abundance of nanoparticles on the surface (Fig. 3b and c). High-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) and energy dispersive X-ray microanalysis (EDX) (Fig. 4a) were performed to examine the high and uniform coverage of nanoparticles. These were identified as 3–5 nm Au nanocrystals (NCs), where the Au-rich clusters appear as bright spots in the HAADF-STEM image. Au atoms that diffuse along the SiNW sidewalls are located mainly at energetically preferred steps of exposed facets or edges, rather than in a perfect crystal plane [19]. Fig. 4b and c clearly shows facets and stacking faults on the SiNW sidewalls, indicating the preferential ⟨1 1 1⟩ growth direction and the presence of stacking faults on the sidewalls of faceted SiNWs. Furthermore, the figures show not only the side facets on the sidewalls consisting of {1 1 1}, {1 0 0}, {1 1 3}, {1 1 5} and {1 1 7} planes, but also stacking faults along the ⟨1 1 1⟩ growth direction based on fast Fourier transform (FFT) diffraction analyses (Fig. 4d and e).

Our results confirm that the highly faceted and tapered morphology could be attributed not only to Au diffusion into the sidewalls of SiNWs from Au–Si catalyst droplets during the VLS process, but also to the enhancement of the VS-dominant process on the sidewalls that creates considerable faceting from lateral growth. However, we observed a predominance of stacking faults along the ⟨1 1 1⟩ growth direction, which has not been commonly reported for ⟨1 1 1⟩-oriented SiNWs. This is because {1 1 1} stacking faults including twin planes can generally be formed in Au-catalyzed Si NWs grown in the ⟨1 1 2⟩ direction [20,21]. More detailed explanations for the formation of facets and stacking faults associated with Au diffusion and lateral growth will be given here.

Faceting on the sidewalls of the SiNWs can be induced by Au decoration [20,21], boron (B) introduction [22] and HCl passivation [15]. According to these studies, the dominant factor could be the presence of impurities on the SiNWs. Since our SiNWs have no dopants, we performed TEM analysis and identified the orientation of the facets in order to study the faceting evolution due to Au diffusion

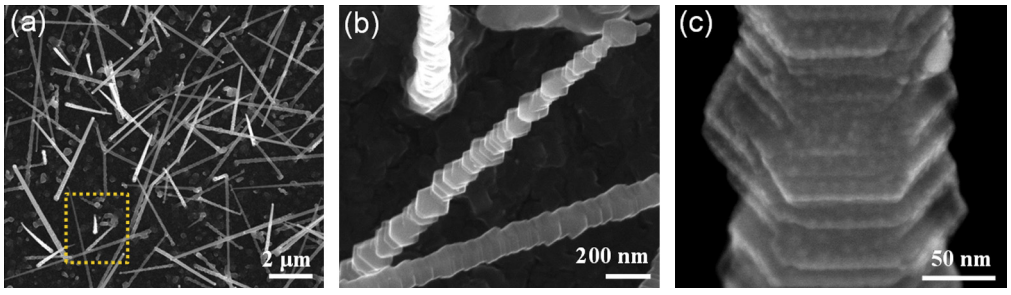

Fig. 3. SEM characterization. (a) SEM image of SiNWs grown on a 2 nm thick Au layer deposited on a Si(1 0 0) substrate using a hot-wall CVD system at 550 °C for 4 h. (b) Enlarged SEM image of squared region in (a). (c) HRSEM image of a SiNW showing the facets and Au NCs on the surface.

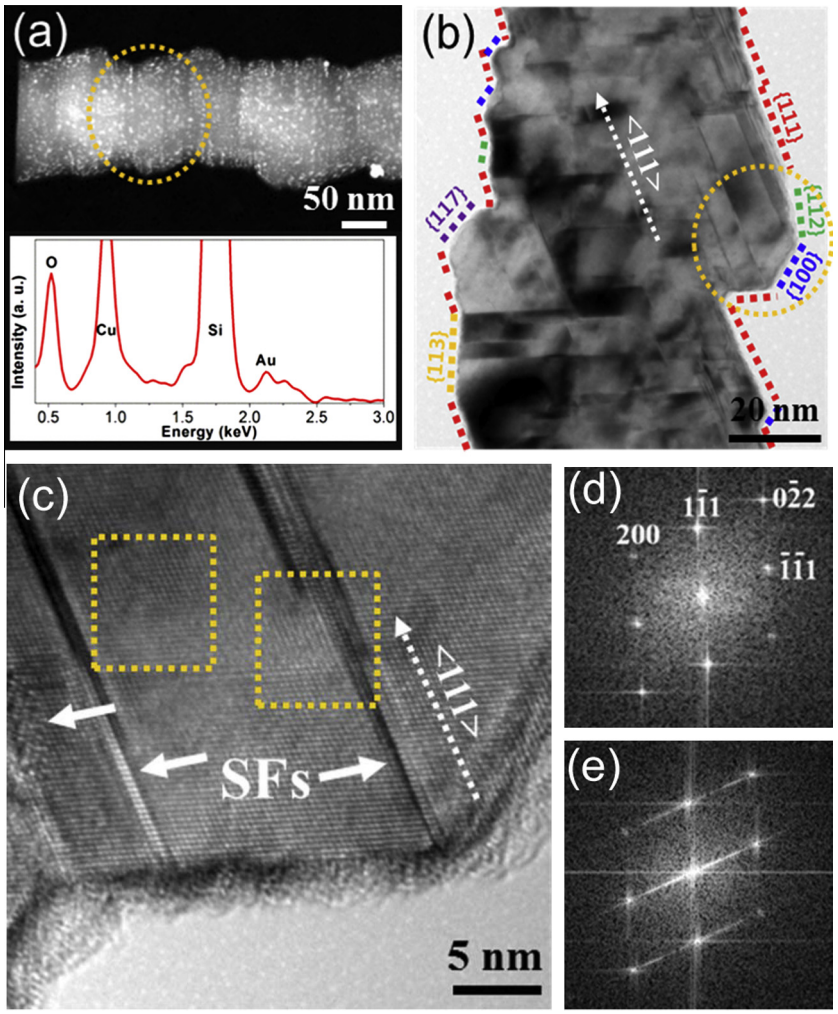

Fig. 4. TEM characterization. (a) STEM image and EDX spectrum of the bottom of a rough SiNW. (b) Bright-field TEM image of circled region in (a). (c) HRTEM image of squared region in (b). (d and e) Selected area electron diffraction patterns of squared region in (c).

as a function of growth time. In the case of SiNW grown for 2 h (Fig. 5a), the facets are mainly composed of long {111} planes and short {100} planes along the {112} sidewalls. However, the {100} planes are gradually converted into {113} planes, and then into {100} planes with increasing exposure time up to 4 h. By increasing growth time up to 9 h, the {100} planes are gradually reconverted into {113} planes, followed by subsequent conversion of both {111} and (100) planes into {112}, {115}, {115} and {117} planes. Our observation of alternating {111} and {100} planes on the sidewalls of SiNWs grown for 2 h is consistent with previous reports [22] where the periodic nanofacets composed of {111} and {100} are generated by enhancing lateral growth on B-doped and Au-decorated sidewalls of the ⟨111⟩-oriented SiNWs. In addition, rougher {111}/{100} facets are formed on the sidewalls by the formation of intermediate {113} planes during lateral growth that result from surface reconstruction on preferentially Au-diffused {113} planes at low silane partial pressure [23].

To further investigate the dependence of growth time on the presence and origin of stacking faults in the SiNWs, we prepared cross-sectional and longitudinal-sectional TEM specimens with FIB ion milling. Fig. 5b–d shows the cross-sectional TEM images of an individual SiNW, indicating that the diameters are 135 nm for a 2 h growth time, 210 nm for a 4 h growth time and 310 nm for a 9 h growth time. The SiNWs consist of a single crystalline Si core region and a defect-laden Si shell region with well-defined {112} side facets, which can be considered as short periodical {111} and {100} steps with atomic layer height [24]. Using high resolution (HR) TEM, we confirmed that all of core regions are highly single-crystalline structures without stacking faults, as shown in Fig. 5b′–d′. On the other hand, the shell regions exhibit defects such as stacking faults and twins (denoted by arrows) that are oriented along both the axial and radial ⟨111⟩ directions, as shown in Figs. 4c and 5b″–d″. We also found that the density of stacking faults and the thickness of the shell regions increase with growth time. In addition, Fig. 5e shows the

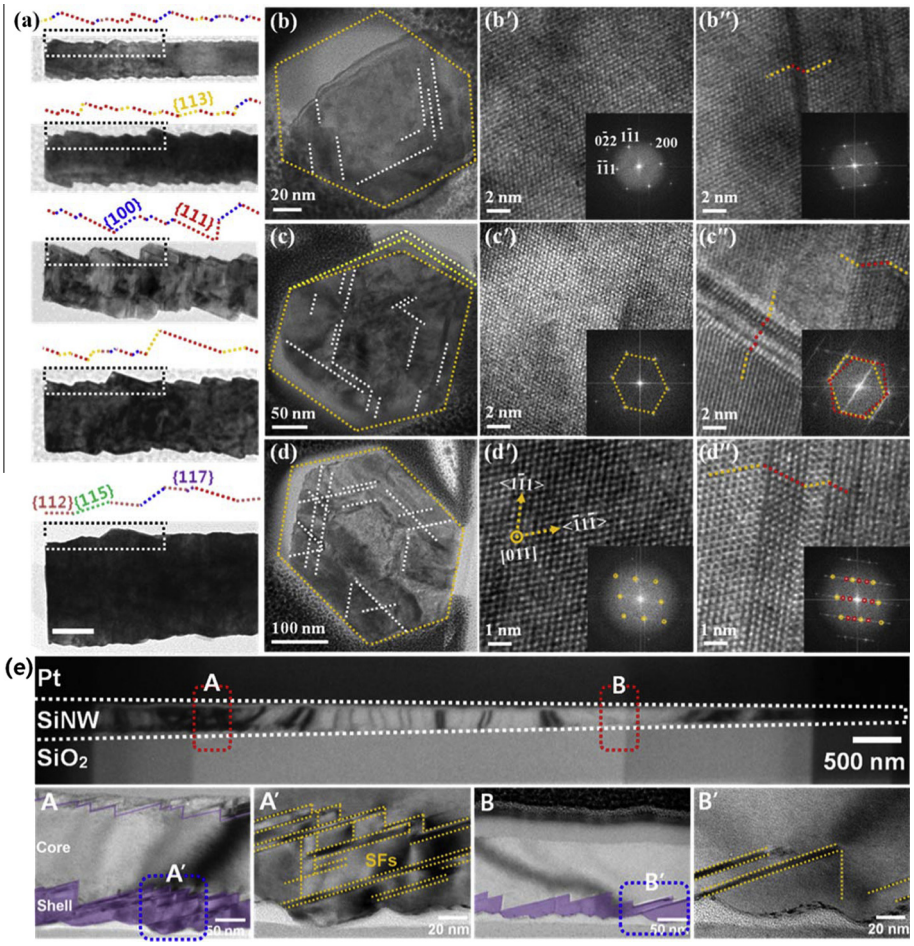

Fig. 5. Faceting and stacking faults analysis. (a) TEM images of SiNW facet orientations grown for 2, 3, 4, 6 and 9 h, respectively. (b–d) Quasi-6-fold cross-sectional TEM images of the SiNW grown for 3, 4 and 6 h, respectively. (b′–d′, and b″–d″) HRTEM images of core and shell regions corresponded to (b–d). (e) Longitudinal TEM images of an individual SiNW grown for 4 h. (A–B′) Enlarged images of squared regions.

longitudinal-sectional TEM images of an individual SiNW, not only demonstrating that the density and thickness of stacking faults (highlighted in purple) gradually decrease along the SiNW shaft, but also exhibiting the similar trend to the roughness and diameter of SiNWs by investigation on enlarged images of each areas. Interestingly, sawtooth facets are observed at the interfacial boundary between the core and shell region. Therefore, we note that the formation of facets and stacking faults obviously depend on Au diffusion and subsequent lateral growth on the sidewalls of $\langle 1\,1\,1\rangle$-oriented SiNWs. Under low silane partial pressure, Au diffusion plays a particularly important role in the formation of facets with the two periodic planes $\{1\,1\,1\}$ and $\{1\,0\,0\}$.

It is especially important to determine where the Au clusters are located on/in the SiNW surface in order to understand the formation of facets and stacking faults. Thus we performed a wet isotropic etching in a mixture of $HF:NH_4F:H_2O$ for 6 h to remove the shell region, consisting of facets and stacking faults on the sidewalls of SiNWs (Fig. 6a). Fig. 6b–e shows less roughness and fewer facets and stacking faults compared with the highly faceted SiNWs. Interestingly, a number of Au nanoparticles (black dots) still appeared on the surface despite the long period of etching (Fig. 6e). Furthermore, the HRTEM images show the abundant presence of Au clusters on the stacking faults along the $\langle 1\,1\,1\rangle$ direction (Fig. 6e and f). Therefore, these stacking faults (yellow arrows) are likely to be bound up with Au clusters (white circles) that are formed on the facets during the lateral growth process (Fig. 6f).

This uncovering of stacking faults and Au clusters in the shell region has important implications with respect to the growth mechanism of the highly faceted and tapered SiNWs. Based on the cross-sectional and longitudinal-sectional TEM results, it is reasonable to assume a growth process in which axial growth (core) is followed by lateral growth (shell) on the sidewalls of the SiNWs. At a low partial pressure (8.2×10^{-3} torr), the supply of Si to the Au catalyst is not sufficient, resulting in an Au-rich region in the phase diagram and excess Au atoms in the droplet. Thus, excess Au atoms diffuse into the SiNW surface by forming an Au–Si eutectic on the surface [25]. They then accelerate lateral growth in the SiNWs, since the Au clusters are an active catalyst for lateral growth. As a result, the surface

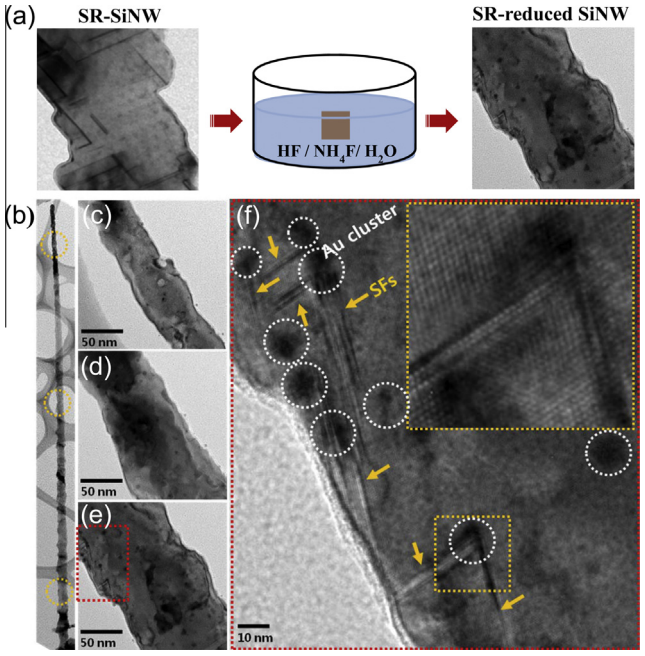

Fig. 6. Au clusters diffusion on the sidewalls of the SiNWs. (a) Illustration of the isotropic etching process for converting surface reconstruction SiNW (SR-SiNW) into surface reconstruction-reduced SiNW (SR-reduced SiNW). (b) TEM images of SR-reduced SiNW. (c–e) Magnified TEM images of the yellow circled regions in (b). (f) High-magnification TEM image of red squared region in (c). (Inset) High-magnification HRTEM of stacking faulted region in (f). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

reconstruction of the sidewalls could induce alternating long {1 1 1} and short {1 0 0} faces during lateral growth. However, the Au atoms that have diffused to the steps of exposed facets or edges readily interact with Si atoms to form Au–Si alloy clusters, which could dislodge from the strong covalently bonded Si crystal structure [26], thus inducing the ⟨1 1 1⟩ stacking faults and the {1 1 1} twinning on/in the facets of NWs during lateral growth. As lateral growth proceeds on the facets of SiNWs via the VS-dominant process, stacking faults are gradually extended to the outer shell region along the ⟨1 1 1⟩ axial and lateral directions.

3.2. Temperature-dependent thermal conductivity measurements of SiNWs

Our well-controlled, highly faceted and stacking-faulted SiNWs should have a better thermal property compared to the VLS-grown and smooth-surfaced NWs, since the thermal conductivity is greatly reduced at the rough facets and stacking faults due to the enhanced phonon-boundary scattering. Furthermore, the highly roughened surface and stacking faults of our SR-SiNWs may also induce enhanced phonon-boundary scattering via coherent phonon (multiple) scattering, as described in previous reports [27–29]. Normally, in the coherent phonon transport regime, we can observe the unusually low thermal conductivity values with an unexpected power law of $\sim T^{\alpha}$ ($1 \leqslant \alpha \leqslant 2$) at low temperature [28,30–32]. Therefore, we systematically measured the thermal conductivities of smooth, SR- and SR-reduced SiNWs at low temperature using a conventional thermal bridge method to further investigate the effects of roughness and stacking faults on coherent phonon transport characteristics. For the final calculation of the thermal conductivities of SR- and SR-reduced NWs (e.g. tapered SiNWs), we employed a modified Fourier's law and introduced effective thermal conductivity $\bar{\kappa}$, as discussed in Section 2.3 to compare the thermal properties of different sizes of tapered SR-SiNWs. As we noticed from longitudinal-sectional images of tapered SR-SiNW from TEM measurements as shown in Figs. 3–5, the thermal conductivity of the SR-SiNW may not be constant along the nanowire. Thus, we believe that more detailed studies including the effect of stacking-fault density of the outer shell region, in which most of defects exist as discussed previously, a lateral thermal conductivity distribution of tapered NW and a new modeling of the anisotropic nanostructure of tapered SiNW, and further measurement study with other techniques, such as spatially resolved thermal resistance mapping measurement using in situ focused e-beam heating techniques, are being studied in our laboratory with the aim of producing a solid explanation for this phenomenon. Moreover, we also considered the uncertainty in measured thermal conductivity of SiNWs. One of the major error sources is the contact thermal resistance between NW and electrodes. To obtain the portion of contact thermal resistance for our set-up and experimental protocol, we measured the thermal resistance of SiNWs with different lengths and diameters [27]. Then, we noticed that the effect of contact thermal resistance was found to be negligible.

Fig. 7a shows the effective thermal conductivity $\bar{\kappa}$ as a function of temperature (25–300 K) for three SR-SiNWs of similar surface morphology and crystal structure but different geometries (see details in Table 1) alongside that of a smooth SiNW ($d \sim 73$ nm) [30]. For the calculation of the thermal conductivity of rough SR-SiNWs using Eq. (8), we took the mean diameter (or radius) of SR-SiNWs and then added the surface roughness contribution to the thermal conductivity with a standard deviation. The root-mean-square (rms) roughness of SR-SiNWs was ~4.5 nm. Accordingly, the effective thermal conductivities of these SR-SiNWs with similar top diameters and different bottom diameters ($d_B \sim 150$, 160 and 195 nm) were determined to be $\sim 19.6 \pm 2.5$, $\sim 16.1 \pm 1.9$ and $\sim 13.0 \pm 1.5$ W m^{-1} K^{-1} at room temperature, respectively. As shown in Fig. 7a, two distinct features of the phonon transport characteristics of SR-SiNWs are observed. First, although SR-SiNWs are thicker than smooth SiNW, the thermal conductivities of SR-SiNWs are lower than that of the smooth SiNW (~25 W m^{-1} K^{-1} at 300 K). To understand this phenomenon, the effects of roughness and facets on the sidewalls of SR-SiNWs were considered. From the previous reports [10,27], we note that the roughness and facets of our

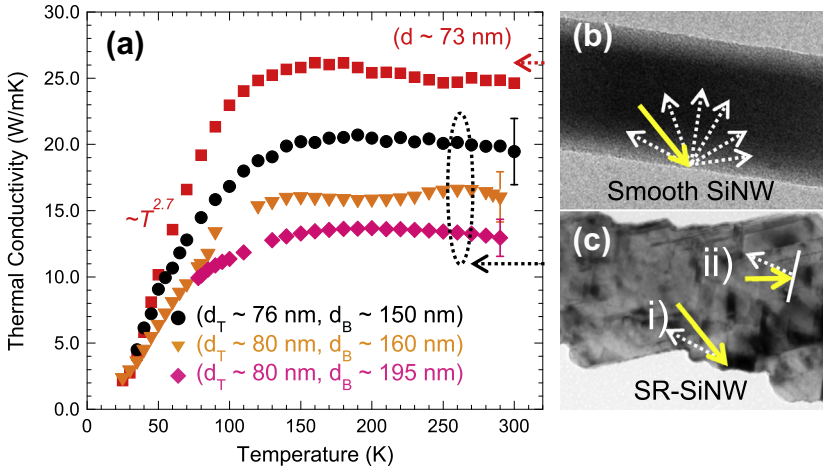

Fig. 7. Temperature-dependent thermal conductivity measurements of SR-SiNW. (a) Thermal conductivities as a function of temperature for smooth and SR-SiNWs. SEM images and schematic diagrams of phonon transport mechanisms in smooth (b) and SR-SiNWs (c).

Table 1
Summary of extracted effective thermal conductivity ($\bar{\kappa}$) of various SiNWs at 300 K. Samples length (m), diameter (nm) at 300 K (W m^{-1} K^{-1}) U-peak (K) $d_T d_B$ Smooth SiNW4.7737324.6160SR-SiNW #15.07615019.6 2.5200SR-SiNW #25.980160

Samples	Length (μm)	Diameter (nm)		$\bar{\kappa}$ at 300 K (W/m K)	U-peak (K)
		d_T	d_B		
Smooth SiNW	4.7	73	73	24.6	160
SR-SiNW #1	5.0	76	150	19.6 ± 2.5	200
SR-SiNW #2	5.9	80	160	16.1 ± 1.9	260
SR-SiNW #3	5.5	80	195	13.0 ± 1.5	200
SR-reduced SiNW	5.0	55	140	39.4 ± 6.3	220

SR-SiNWs may have contributed to higher rates of phonon scattering, leading to further enhanced phonon-boundary scattering that results in greatly reduced thermal conductivity. Fig. 7b and c shows the schematic diagrams of the phonon transport mechanism in smooth SiNWs and SR-SiNWs, respectively. In smooth SiNWs, mainly diffusive boundary scattering occurs, where phonons scatter (white-dot arrows in Fig. 7) from the surface in any direction irrespective of the angle of the incident phonon (yellow[2] arrows in Fig. 7). In the diffusive regime, the size of SiNWs limits the phonon-boundary scattering. On the other hand, the roughness and facets of SR-SiNWs behave like secondary phonon scattering phases (Fig. 7c), resulting in the enhancement of phonon-boundary scattering via diffuse reflection and backscattering [1,2,4,5,10,27]. Consequently, the thermal conductivity of our SR-SiNWs could be reduced by a roughness- and facet-induced phonon-boundary scattering on the sidewalls. Our experimental results are in good agreement with previous reports on rough and faceted SiNWs [2,4,5,10,27].

The other notable feature is that the thermal conductivity of SR-SiNWs is smaller for NWs of larger base, which is not consistent with previous reports [1–3,5,30,33]. Typically, when the NWs have a similar surface morphology and crystal structure, the thermal conductivity decreases with decreasing NW thickness because of the enhanced phonon-boundary scattering at the surface. This abnormal phonon transport characteristic of SR-SiNWs can be explained by stacking-faults-induced phonon-boundary scattering. As discussed above, the diffuse reflection and backscattering can take place at the outer shell region of SR-SiNWs, since the stacking faults could contribute to higher rates of phonon-boundary scattering (Fig. 7c). In our growth model, stacking faults were formed at the outer shell region of SiNWs, as shown in Fig. 5. As a result, the number of stacking faults for thicker SR-SiNWs is much higher relative to those for thinner ones, indicating that the thermal conductivities of SR-SiNWs are inversely proportional to the thickness of SiNWs. Consequently, we found that the stacking-fault-induced phonon-boundary scattering dominates over other phonon scattering mechanisms.

To further elucidate the effects of surface reconstruction (e.g. roughness and stacking faults) on the suppression of thermal conductivity in SR-SiNWs, the outer shell region of the SR-SiNWs was wet-chemically-etched away (Fig. 6a). As shown in Fig. 8a, the thermal conductivity of SR-reduced SiNW, which had a d_T of ~55 nm and a d_B of ~140 nm, is two to three times higher relative to that for SR-SiNWs of comparable thickness. Thus we see decreased phonon-boundary scattering with less roughness

[2] For interpretation of color in Fig. 7, the reader is referred to the web version of this article.

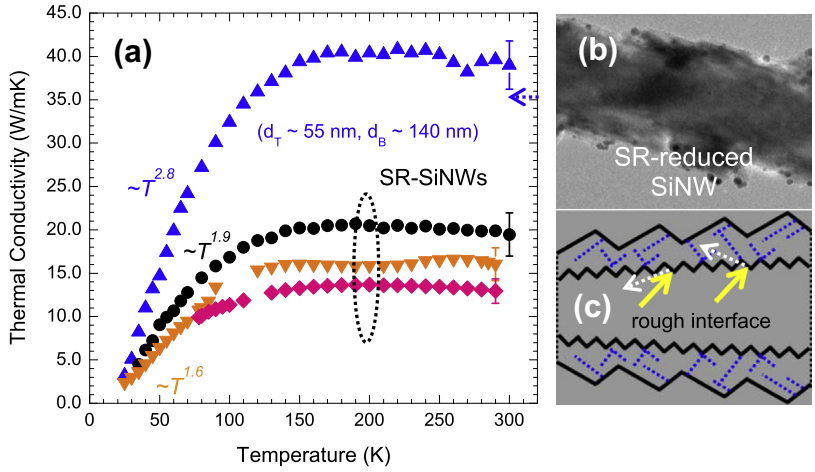

Fig. 8. Temperature-dependent thermal conductivity measurements of SR-reduced SiNW. (a) Thermal conductivities as a function of temperature for SR-reduced and SR-SiNWs. (b) SEM image of SR-reduced SiNW using a HF:NH_4F:H_2O solution for 6 h at room temperature. (c) Schematic illustration of phonon scattering at rough interface in SR-SiNWs. (White-dot arrows: scattered phonons; yellow arrows: incident phonons.) The average thermal conductivity with a standard deviation caused by surface roughness at 300 K is also indicated in the plot. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

and fewer stacking faults. It clearly indicates that the phonon transport characteristics can be successfully controlled by surface reconstruction in SiNWs. Surprisingly, however, even if the phonon-boundary scattering has been significantly enhanced via diffuse reflection and backscattering at rough surface and stacking faults, our measured thermal conductivity values of SR-SiNWs are still considerably lower than that predicted from Casimir's limit for given NW diameters (up to 195 nm) (Fig. 8b and c). This phenomenon can be considered as coherent phonon transport characteristics [3,28,30–32,34]. In a coherent phonon transport regime, we can observe that the phonon transport shows the frequency-dependent phonon scattering with unexpected power law of $\sim T^{\alpha}$ $(1 \leqslant \alpha \leqslant 2)$ at low temperature [3,32,34]. Interestingly, our SR-SiNWs also show the unexpected power law of $\sim T^{\alpha}$ $(1.6 \leqslant \alpha \leqslant 1.9)$ in the temperature range of 25–60 K, as shown in Fig. 8a, distinct from the Debye $\sim T^3$ behavior. To understand this coherent phonon transport mechanisms in SR-SiNWs, we invoke the low temperature limit of a Debye model with strong boundary scattering, which can be described by the following equation derived from the kinetic theory of thermal conductivity on a three-dimensional phonon gas $(k = 1/3 \sum Cv\lambda)$ [32,34]:

$$k = \frac{k_B v}{2\pi^2}\left(\frac{k_B T}{\hbar v}\right)^3 \int_0^{\infty} \frac{x^4 e^x \lambda}{(e^2-1)^2} dx \qquad (9)$$

where k_B is the Boltzmann constant, $\hbar$ is the reduced Planck constant, v is the averaged sound velocity and $x = \hbar\omega/k_B T$. Wang et al. showed the frequency-dependent phonon transport with $\kappa \propto T^2$ and $\lambda \propto \omega^{-1}$ trends (if $\lambda \propto \omega^x$, then $\kappa \propto T^{3+x}$, $-2 \leqslant x \leqslant 0$)) in nanocrystalline Si by using Eq. (9) [34]. With this regime, we clearly notice that our SR-SiNWs exhibit coherent phonon transport characteristics with an anomalous power law of $\sim T^{\alpha}$ $(1.6 \leqslant \alpha \leqslant 1.9)$, as shown in Fig. 8a. To understand the observed coherent phonon transport behavior in SR-SiNWs, we considered the coherent (multiple) phonon scattering suggested by the Sinha research group [31,32]. They have shown both experimentally and theoretically coherent phonon scattering at grain boundaries and rough surface in Si inverse opals and rough SiNWs [28,31,32]. Similarly, we hypothesize that coherent (multiple) phonon scattering can be induced by both rough surface and stacking faults in SR-SiNWs, leading to frequency-dependent phonon transport characteristics, resulting in the severely reduced thermal conductivity values for the given NW diameters. As compared with smooth and SR-reduced SiNWs in Figs. 7a and 8a, it can be clearly seen that the phonon transport follows the frequency-independent model, which fits the Debye T^3 well, since the impacts of roughness and stacking faults are quite low on coherent phonon scattering. Our results show that the roughness and stacking faults play a dominant role in coherent phonon scattering in SR-SiNWs. However, to establish the correct phonon scattering mechanism and model, further detailed experimental and theoretical analysis of the effects of roughness parameters (e.g. correlation length, rms), rough interface and stacking faults on coherent phonon heat conduction should be considered.

4. Conclusions

We have reported a new method for producing high-roughness and stacking-faulted SiNWs to enhance phonon-boundary scattering. The faceting and the formation of stacking faults are strongly dependent on Au diffusion and the subsequent lateral growth on the sidewalls of SiNWs. Thus we can easily control the surface morphology and crystal structure by an in situ, Au-catalyzed, one-step

combined VLS–VS process during SiNW growth without additional processing such as wet chemical etching, doping or alloying. We demonstrated that our well-controlled, highly faceted and stacking-faulted SiNWs show an increase in thermal conductivity along their length due to a progressive decrease of both roughness and stacking fault density, despite a tapering down of the diameter. Furthermore, we also observed that our SR-SiNWs exhibit unusually low thermal conductivity values with unexpected power law of $\sim T^{\alpha}$ ($1.6 \leqslant \alpha \leqslant 1.9$) in the temperature range of 25–60 K for the range of diameters studied. These abnormal behaviors are consistent with a frequency-dependent model caused by coherent (multiple) phonon scattering at the rough surface and stacking faults on SR-SiNWs. Based on this study, we believe that our facile approach may be extended to other promising one-dimensional TE materials and devices to enhance their TE performance.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.actamat.2013.11.042.

References

[1] Li DY, Wu YY, Kim P, Shi L, Yang PD, Majumdar A. Appl Phys Lett 2003;83:2934.
[2] Park YH, Kim J, Kim H, Kim I, Lee KY, Seo D, et al. Appl Phys A – Mater 2011;104:7.
[3] Chen R, Hochbaum AI, Murphy P, Moore J, Yang PD, Majumdar A. Phys Rev Lett 2008:101.
[4] Hochbaum AI, Chen RK, Delgado RD, Liang WJ, Garnett EC, Najarian M, et al. Nature 2008;451:163.
[5] Boukai AI, Bunimovich Y, Tahir-Kheli J, Yu JK, Goddard WA, Heath JR. Nature 2008;451:168.
[6] Chen J, Zhang G, Li BW. Nano Lett 2010;10:3978.
[7] Hsieh TY, Yang JY. J Appl Phys 2010:108.
[8] Paul A, Klimeck G. Appl Phys Lett 2011:98.
[9] Donadio D, Galli G. Nano Lett 2010;10:847.
[10] Sansoz F. Nano Lett 2011;11:5378.
[11] Li YD, Buddharaju K, Tinh BC, Singh N, Lee SJ. IEEE Electr Device Lett 2012;33:715.
[12] Li Y, Buddharaju K, Singh N, Lo GQ, Lee SJ. IEEE Electr Device Lett 2011;32:674.
[13] Hannon JB, Kodambaka S, Ross FM, Tromp RM. Nature 2006;440:69.
[14] den Hertog MI, Rouviere JL, Dhalluin F, Desre PJ, Gentile P, Ferret P, et al. Nano Lett 2008;8:1544.
[15] Oehler F, Gentile P, Baron T, Ferret P, Den Hertog M, Rouviere J. Nano Lett 2010;10:2335.
[16] Seo DW, Kim GS, Lee CY, Lee SY, Hyung JH, Choi CJ, et al. J Appl Phys 2012;111:034301.
[17] Lee CY, Kim GS, Lee SY, Kim TH, Seo DW, Lee SK. J Nanosci Nanotechnol 2011;11:6946.
[18] Shi L, Li DY, Yu CH, Jang WY, Kim DY, Yao Z, et al. J Heat Transf – Trans ASME 2003;125:1209.
[19] Ashcroft NW, Mermin NW. Solid state physics. Thomson Learning, Inc.; 1976.
[20] Davidson FM, Lee DC, Fanfair DD, Korgel BA. J Phys Chem C 2007;111:2929.
[21] Lopez FJ, Hemesath ER, Lauhon LJ. Nano Lett 2009;9:2774.
[22] Li F, Nellist PD, Lang C, Cockayne DJH. Acs Nano 2010;4:632.
[23] Xu T, Nys JP, Addad A, Lebedev OI, Urbieta A, Salhi B, et al. Phys Rev B 2010:81.
[24] Grein CH. J Cryst Growth 1997;180:54.
[25] Kawashima T, Mizutani T, Nakagawa T, Torii H, Saitoh T, Komori K, et al. Nano Lett 2008;8:362.
[26] Hiraki A. Surf Sci Rep 1984;3:357–412.
[27] Lim JW, Hippalgaonkar K, Andrews SC, Majumdar A, Yang PD. Nano Lett 2012;12:2475.
[28] Sadhu J, Sinha S. Phys Rev B 2011:84.
[29] Wang ZJ, Alaniz JE, Jang WY, Garay JE, Dames C. Nano Lett 2011;11:2206.
[30] Lim J, Hippalgaonkar K, Andrews SC, Majumdar A, Yang P. Nano Lett 2012;12:2475.
[31] Sadhu J, Seong M, Sinha S. J Comput Electron 2012;11:1.
[32] Ma J, Parajuli BR, Ghossoub MG, Mihi A, Sadhu J, Braun PV, et al. Nano Lett 2013;13:618.
[33] Bui CT, Xie RG, Zheng MR, Zhang QX, Sow CH, Li BW, et al. Small 2012;8:738.
[34] Wang ZQ, Xie RG, Bui CT, Liu D, Ni XX, Li BW, et al. Nano Lett 2011;11:113.